

DUAL GATE DIELECTRIC CONSTRUCTION

Abstract of the Disclosure

Dual gate dielectric constructions and methods therefor are disclosed for different regions on an integrated circuit. In the illustrated embodiment, gate dielectrics in memory array regions of the chip are formed of silicon oxide, while the gate dielectric in the peripheral region comprises a harder material, specifically silicon nitride, and has a lesser overall equivalent oxide thickness. The illustrated peripheral gate dielectric has an oxide-nitride-oxide construction. The disclosed process includes forming silicon nitride over the entire chip followed by selectively etching off the silicon nitride from the memory array region, without requiring a separate mask as compared to conventional processes. After the selective etch, oxide is grown over the entire chip, growing differentially thicker in the memory array region.

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